In the Claims:

A. Kindly cancel Claims 5 and 15, without prejudice.

B. Kindly amend Claims 1, 6, 11, and 16, as follows.

1. **(currently amended)** A method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of:

providing a semiconductor substrate having a Cu surface formed in a via;

providing a chemical solution;

electroplating the Cu surface in the chemical solution thereby forming said a Cu-Zn alloy fill in the via and on the Cu surface,

wherein said electroplating comprises using an electroplating apparatus,

wherein said electroplating apparatus comprises:

(a) a cathode-wafer;

(b) an anode;

(c) electroplating vessel; and

(d) a voltage source, and

wherein the cathode-wafer comprises the Cu surface,

rinsing the Cu-Zn alloy fill in a solvent;

drying the Cu-Zn alloy fill under a gaseous flow;

annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming a reduced-oxygen Cu-Zn alloy fill having a uniform zinc distribution;

planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and

completing formation of the semiconductor device.

2. **(original)** A method, as recited in Claim 1,

wherein the chemical solution is nontoxic and aqueous, and

wherein the chemical solution comprises:

at least one zinc (Zn) ion source for providing a plurality of Zn ions;

at least one copper (Cu) ion source for providing a plurality of Cu ions;

at least one complexing agent for complexing the plurality of Cu ions;

at least one pH adjuster;

at least one wetting agent for stabilizing the chemical solution, all being dissolved in a volume of deionized (DI) water.

3. **(original)** A method, as recited in Claim 2,

wherein the at least one zinc (Zn) ion source comprises at least one zinc salt selected from a group consisting essentially of zinc acetate ($(CH_3CO_2)_2Zn$), zinc bromide ($ZnBr_2$), zinc carbonate hydroxide ($ZnCO_3 \cdot 2Zn(OH)_2$), zinc dichloride ($ZnCl_2$), zinc citrate ($(O_2CCH_2C(OH)(CO_2)CH_2CO_2)_2Zn_3$), zinc iodide ($ZnI_2$), zinc L-lactate ($(CH_3CH(OH)CO_2)_2Zn$), zinc nitrate ($Zn(NO_3)_2$), zinc stearate ($(CH_3(CH_2)_{16}CO_2)_2Zn$), zinc sulfate ($ZnSO_4$), zinc sulfide ($ZnS$), zinc sulfite ($ZnSO_3$), and their hydrates.

4. **(original)** A method, as recited in Claim 2,

wherein the at least one copper (Cu) ion source comprises at least one copper salt selected from a group consisting essentially of copper(I) acetate (CH_3CO_2Cu), copper(II) acetate ($(CH_3CO_2)_2Cu$), copper(I) bromide ($CuBr$), copper(II) bromide ($CuBr_2$), copper(II) hydroxide ($Cu(OH)_2$), copper(II) hydroxide phosphate ($Cu_2(OH)PO_4$), copper(I) iodide (CuI), copper(II) nitrate ($(CuNO_3)_2$), copper(II) sulfate ($CuSO_4$), copper(I) sulfide (Cu_2S), copper(II) sulfide (CuS), copper(II) tartrate ($(CH(OH)CO_2)_2Cu$), and their hydrates.

5. **(canceled)**

6. **(currently amended)** A method, as recited in Claim ~~5~~1,

~~wherein the cathode-wafer comprises the Cu surface, and~~

wherein the anode comprises at least one material selected from a group consisting essentially of copper (Cu), a copper-platinum alloy (Cu-Pt), titanium (Ti), platinum (Pt), a titanium-platinum alloy (Ti-Pt), an anodized copper-zinc alloy

(Cu-Zn, i.e., brass), a platinized titanium (Pt/Ti), and a platinized copper-zinc (Pt/Cu-Zn, i.e., platinized brass).

7. **(original)** A method, as recited in Claim 1,
wherein said semiconductor substrate further comprises a barrier layer formed in the via under said Cu surface, and
wherein the barrier layer comprises at least one material selected from a group consisting essentially of titanium silicon nitride ($Ti_xSi_yN_z$), tantalum nitride (TaN), and tungsten nitride (W_xN_y).

8. **(original)** A method, as recited in Claim 7,
wherein said semiconductor substrate further comprises an underlayer formed on the barrier layer,
wherein said underlayer comprises at least one material selected from a group consisting essentially of tin (Sn) and palladium (Pd), and
wherein said Cu surface is formed over said barrier layer and on said underlayer.

9. **(original)** A method, as recited in Claim 8,
wherein said underlayer comprises a thickness range of approximately 15 Å to approximately 50 Å,
wherein said barrier layer comprises a thickness range of approximately 30 Å to approximately 50 Å,
wherein said Cu surface comprises a thickness range of approximately 50 Å to approximately 70 Å, and
wherein said Cu-Zn alloy fill comprises a thickness range of approximately 300 Å to approximately 700 Å.

10. **(original)** A method, as recited in Claim 1,
wherein the annealing steps are performed in a temperature range of approximately 150°C to approximately 450°C, and
wherein the annealing steps are performed for a duration range of approximately 0.5 minutes to approximately 60 minutes.

11. **(currently amended)** A semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by a method comprising the steps of:

providing a semiconductor substrate having a Cu surface formed in a via;

providing a chemical solution;

electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface;

<u>wherein said electroplating comprises using an electroplating apparatus, wherein said electroplating apparatus comprises:</u>

<u>(a) a cathode-wafer;</u>

<u>(b) an anode;</u>

<u>(c) electroplating vessel; and</u>

<u>(d) a voltage source, and</u>

<u>wherein said cathode-wafer comprises the Cu surface,</u>

rinsing the Cu-Zn alloy fill in a solvent;

drying the Cu-Zn alloy fill under a gaseous flow;

annealing the Cu-Zn alloy fill formed in the via and on the Cu surface, thereby forming a reduced-oxygen Cu-Zn alloy fill <u>having a uniform zinc distribution</u>;

planarizing the reduced-oxygen Cu-Zn alloy fill and the Cu surface, thereby completing formation of a reduced-oxygen Cu-Zn alloy filled dual-inlaid interconnect structure; and

completing formation of the semiconductor device.

12. **(original)** A device, as recited in Claim 11,

wherein the chemical solution is nontoxic and aqueous, and

wherein the chemical solution comprises:

at least one zinc (Zn) ion source for providing a plurality of Zn ions;

at least one copper (Cu) ion source for providing a plurality of Cu ions;

at least one complexing agent for complexing the plurality of Cu ions;

at least one pH adjuster;

at least one wetting agent for stabilizing the chemical solution, all being dissolved in a volume of deionized (DI) water.

13. **(original)** A device, as recited in Claim 12,
wherein the at least one zinc (Zn) ion source comprises at least one zinc salt selected from a group consisting essentially of zinc acetate ($(CH_3CO_2)_2Zn$), zinc bromide ($ZnBr_2$), zinc carbonate hydroxide ($ZnCO_3 \cdot 2Zn(OH)_2$), zinc dichloride ($ZnCl_2$), zinc citrate ($(O_2CCH_2C(OH)(CO_2)CH_2CO_2)_2Zn_3$), zinc iodide ($ZnI_2$), zinc L-lactate ($(CH_3CH(OH)CO_2)_2Zn$), zinc nitrate ($Zn(NO_3)_2$), zinc stearate ($(CH_3(CH_2)_{16}CO_2)_2Zn$), zinc sulfate ($ZnSO_4$), zinc sulfide ($ZnS$), zinc sulfite ($ZnSO_3$), and their hydrates.

14. **(original)** A device, as recited in Claim 12,
wherein the at least one copper (Cu) ion source comprises at least one copper salt selected from a group consisting essentially of copper(I) acetate (CH_3CO_2Cu), copper(II) acetate ($(CH_3CO_2)_2Cu$), copper(I) bromide ($CuBr$), copper(II) bromide ($CuBr_2$), copper(II) hydroxide ($Cu(OH)_2$), copper(II) hydroxide phosphate ($Cu_2(OH)PO_4$), copper(I) iodide (CuI), copper(II) nitrate hydrate ($(CuNO_3)_2$), copper(II) sulfate ($CuSO_4$), copper(I) sulfide (Cu_2S), copper(II) sulfide (CuS), copper(II) tartrate ($(CH(OH)CO_2)_2Cu$), and their hydrates.

15. **(canceled)**

16. **(currently amended)** A device, as recited in Claim 11~~15~~,
~~wherein the cathode-wafer comprises the Cu surface, and~~
wherein the anode comprises at least one material selected from a group consisting essentially of copper (Cu), a copper-platinum alloy (Cu-Pt), titanium (Ti), platinum (Pt), a titanium-platinum alloy (Ti-Pt), an anodized copper-zinc alloy (Cu-Zn, i.e., brass), a platinized titanium (Pt/Ti), and a platinized copper-zinc (Pt/Cu-Zn, i.e., platinized brass).

17. **(original)** A device, as recited in Claim 11,

wherein said semiconductor substrate further comprises a barrier layer formed in the via under said Cu surface, and

wherein the barrier layer comprises at least one material selected from a group consisting essentially of titanium silicon nitride ($Ti_xSi_yN_z$), tantalum nitride (TaN), and tungsten nitride (W_xN_y).

18. **(original)** A device, as recited in Claim 17,

wherein said semiconductor substrate further comprises an underlayer formed on the barrier layer,

wherein said underlayer comprises at least one material selected from a group consisting essentially of tin (Sn) and palladium (Pd), and

wherein said Cu surface is formed over said barrier layer and on said underlayer.

19. **(original)** A device, as recited in Claim 18,

wherein said underlayer comprises a thickness range of approximately 15 Å to approximately 50 Å,

wherein said barrier layer comprises a thickness range of approximately 30 Å to approximately 50 Å,

wherein said Cu surface comprises a thickness range of approximately 50 Å to approximately 70 Å, and

wherein said Cu-Zn alloy fill comprises a thickness range of approximately 300 Å to approximately 700 Å.

20. **(original)** A semiconductor device, having a first interim reduced-oxygen copper-zinc (Cu-Zn) alloy fill formed on a copper (Cu) surface and a second interim reduced-oxygen Cu-Zn alloy fill formed on a Cu-fill, both films being formed by electroplating the Cu surface and the Cu-fill, respectively, in a chemical solution, comprising:

a semiconductor substrate having a via; and

an encapsulated dual-inlaid interconnect structure formed and disposed in said via, said interconnect structure comprising:

at least one Cu surface formed in said via;

a first interim reduced-oxygen Cu-Zn alloy fill formed and disposed on the at least one Cu surface;

a Cu-fill formed and disposed on said interim reduced-oxygen Cu-Zn alloy fill; and

a second interim reduced-oxygen Cu-Zn alloy fill formed and disposed on the Cu-fill.